from a requesting processor, issuing a request for a block of data to one or more other processors and memory, each copy of the block of data being associated with state information indicating whether the copy is valid or invalid;

in each of the processors and memory that receive the request, checking to determine whether a valid copy of the block of data exists; and

returning a valid copy of the requested data from one of the other processors or memory such that only the processor or memory having the valid copy of the data block responds to the request,

as recited in claim 1. Although the patent to Chang refers to "snooping," Chang is concerned with idle cycles associated with the process of invalidating TLB entries in non-initiating processors, and not with performance issues associated with requests for data, to which claims 1-20 are directed.

Chang does not discuss responding to requests for data in the passages indicated in the Final Office Action. In particular, Chang does not disclose "returning a valid copy of the requested data from one of the other processors or memory such that ***only the processor or memory*** having ***the valid copy*** of the data block ***responds*** to the request," (emphasis added) as recited in claim 1. Further, Chang does not disclose "each of the processors and the shared memory being responsive to a request to check itself for a valid copy of a requested block such that ***only the processor or shared memory having the valid copy responds*** to the request for the requested block," (emphasis added) as recited in claims 9 and 19.

Instead, Chang's data processing system 8, allows snooping processors to continue processing instructions when a synchronization instruction is received. Column 11, lines 39-43. Chang's data processing system 8 includes a processor 10 providing a response to an initiating processor 10a initiating TLB entry invalidation, indicating that the processor's 10 bus interface unit 30 has verified that all marked instructions have drained from the snooping processor. Col. 11, lines 46-53.

The passage pointed out in the Final Office Action as including the feature of "***only the processor or shared memory having the valid copy responds*** to the request" states only that, after the instructions received from the initiating processor 10a are completed, the snooping processor 10 may provide "an appropriate response (which may be no response in certain communication protocols)." The passage does not address receiving a request for data. This passage is directed to responding to instructions received to invalidate TLB entries.

Thus, Chang does not anticipate the invention claimed by independent claims 1, 9 and 19. Therefore, claims 1, 9 and 19, and their dependent claims 2-7, 10-18 and 20 are allowable over Chang. Although Applicant does not agree with all characterizations in the Final Office Action of October 10, 2001, Applicant reserves those arguments for another time.

CONCLUSION

As all of the outstanding rejections have been traversed and all of the claims are believed to be in condition for allowance, the Applicants respectfully request issuance of a Notice of Allowability. If the undersigned attorney can assist in any matters regarding examination of this application, the Examiner is encouraged to call at the number listed below.

Respectfully submitted,
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Version with markings to show changes made

Preferably, the request queues communicate requests via a high-speed internal address bus or switch 223 (referred to generally as a "bus" or "control path interconnect"). Each of the processors and [memory] main memory devices are capable of storing a copy of a requested data block. Therefore, each has a corresponding destination buffer (e.g., queues 224, 226, 228, 230) in the memory controller for receiving memory requests from the buss 223. The buffers for receiving requests destined for processors are referred to as snoop queues (e.g., SnoopQs 224 and 226).